


IN THE CLAIMS:

Please amend the claims to read as follows:

13 (currently amended): A method of fabricating an integrated circuit chip comprising:

 processing a semiconductor substrate to form a gate array architecture of transistors in the substrate, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites ~~to form~~ at least one forming both N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

14 (original): The method of claim 13, wherein said semiconductor substrate comprises a silicon substrate.

15 (original): The method of claim 14, wherein processing said silicon substrate to form a gate array architecture comprises:

forming said partially overlying polysilicon landings so that said landings for the smaller and larger transistors are not connected.

16 (original): The method of claim 15, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

17 (original): The method of claim 16, wherein the ratio between the capacitance of the larger and smaller relatively sized transistors is on the order of one-third.

18 (currently amended): The method of claim 15, and further comprising:

forming ~~a metallization~~ an interconnect overlying said gate array architecture.

19 (currently amended): The method of claim 18, wherein forming ~~a metallization~~ an interconnect comprises forming ~~a metallization~~ an interconnect that connects the transistors of the gate array architecture to form a flip-flop having internal clock buffers.

20 (currently amended): The method of claim 19, where in forming a ~~metallization~~ an interconnect comprises forming an interconnect that connects the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

27 (new): The method of claim 13, wherein said transistors are formed in said gate array architecture so that an interconnect disposed thereon is capable of connecting said smaller transistors to form internal clock buffers.

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